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8086 microprocessor Architecture

- Subject: Microprocessor
- Department : Computer Engineering
- Year : Second year
- Semester : IV

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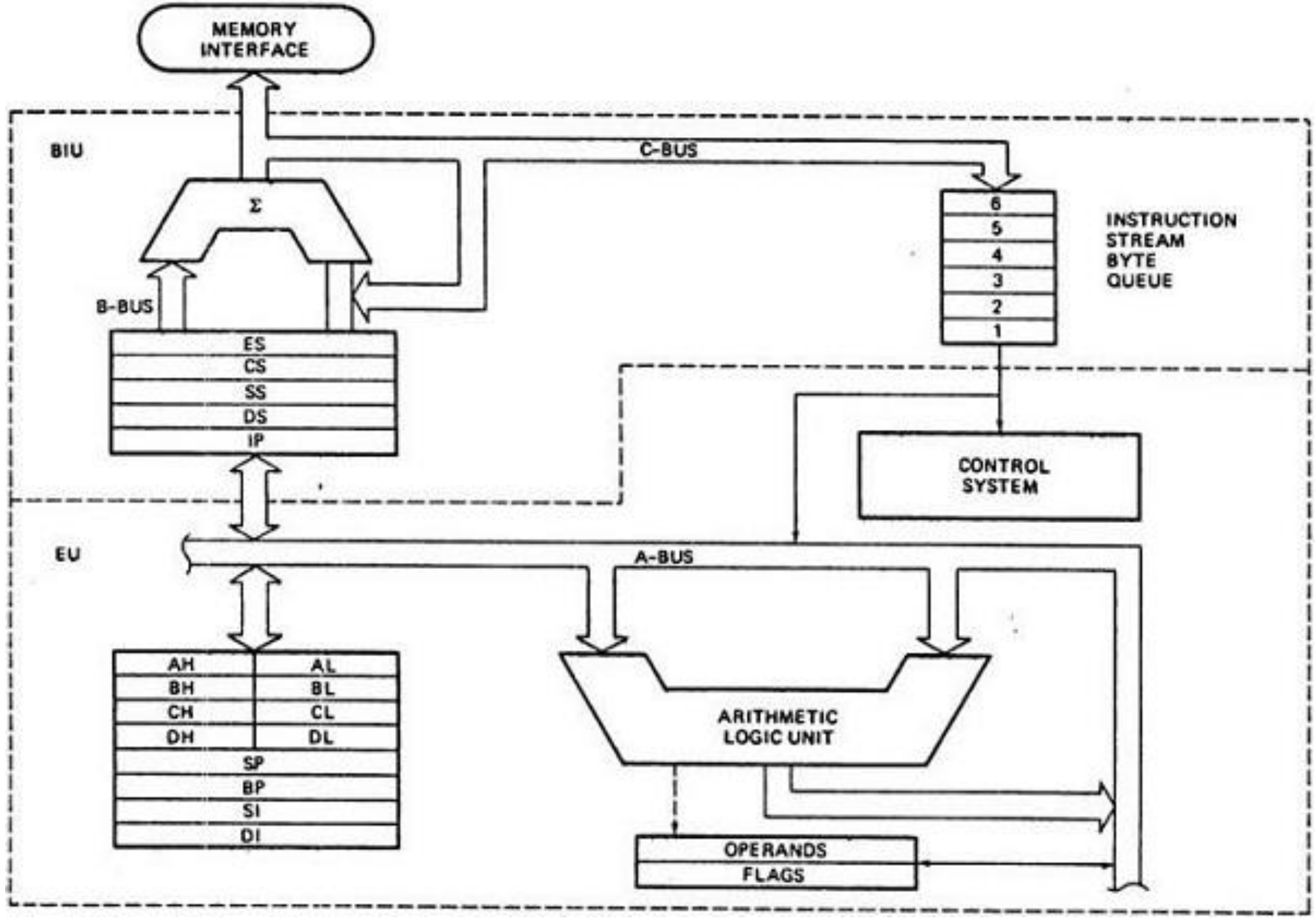

MEMORY INTERFACE
BIU
C-BUS
Σ
B-BUS
6
5
4
3
2
1
INSTRUCTION STREAM BYTE QUEUE
ES
CS
SS
DS
IP
CONTROL SYSTEM
EU
A-BUS
AH
AL
BH
BL
CH
CL
DH
DL
SP
BP
SI
DI
ARITHMETIC LOGIC UNIT
OPERANDS
FLAGS

8086 Microprocessor

- **16 bits microprocessor**
- **16 bits data bus**
- **20 bits address bus**
- **CISC architecture**
- **1 MB physical address space**

8086 Microprocessor

- BIU : Bus Interface Unit.
- Address generating circuit.
- 6 instructions prefetch queue.
- 4 segments of 64 KB of separate I/O space.
- 8 general 16-bit registers.

8086 Microprocessor

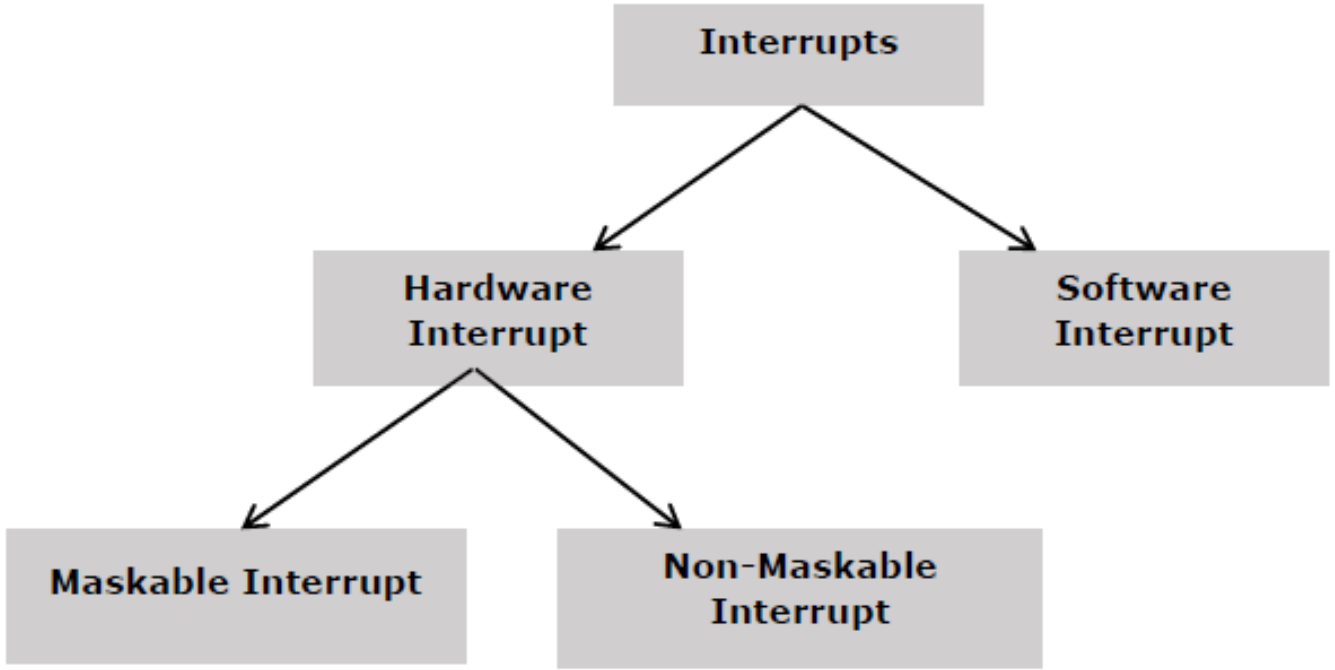
- **EU Execution Unit**
- 32-bits ALU
- 8 bit registers paired into 16 bits general purpose register- AX,BX,CX & DX
- Special purpose register- stack pointer, base pointer, source index & destination index

8086 Microprocessor

- 40 pins dual in line package .
- High speed .
- Powerful instruction set.
- 2 operating modes- minimum mode and maximum mode.
- It can support 64k I/O ports.
- Memory segmentation
- Memory banking

8086 Microprocessor

- 2 hardware interrupts- NMI & INTR
- 256 software interrupts



Aspect	Non-Maskable Interrupt (NMI)	Interrupt (INTR)
Triggering Factor	Caused by critical hardware failures or exceptional conditions that require immediate attention	Initiated by external hardware devices or software instructions based on specific events or conditions
Priority	Higher priority than INTR, cannot be disabled or masked	Lower priority compared to NMI, can be disabled or masked
Purpose	Typically used for handling critical system errors or emergencies, such as power failure detection or hardware malfunctions	Used for handling regular events or tasks, such as I/O operations or timer events
Response Time	Immediate response is expected to address critical issues	Response may vary based on the priority of the interrupt and the current processor state
Masking and Handling	Cannot be disabled or masked, usually directly handled by dedicated hardware	Can be disabled or masked temporarily to prioritize other tasks, handled by the interrupt controller and processor interrupt handling mechanism
Examples	Power failure, memory parity errors, hardware malfunctions	Keyboard input, timer overflow, I/O device request


thank you!